UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF MINNESOTA

REGENTS OF THE UNIVERSITY OF MINNESOTA Plaintiff, v. AT&T MOBILITY LLC et al., Defendants.	Civil Action No. 0:14-cv-04666 JRT/TNL
REGENTS OF THE UNIVERSITY OF MINNESOTA Plaintiff. v. SPRINT SPECTRUM L.P., et al., Defendants	Civil Action No. 0:14-cv-04669 JRT/TNL

REGENTS OF THE UNIVERSITY OF MINNESOTA Plaintiff. v. T-MOBILE USA, INC. et al., Defendants.	Civil Action No. 0:14-cv-04671 JRT/TNL
REGENTS OF THE UNIVERSITY OF MINNESOTA Plaintiff. v. CELLCO PARTNERSHIP D/B/A VERIZON WIRELESS et al., Defendants.	Civil Action No. 0:14-cv-04672 JRT/TNL

DEFENDANTS'
OPENING CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

PAGE(S)

TABLE OF ABBREVIATIONS

Abbreviation	Keyword	Exhibit Number
'185	USP 8,718,185	
'230	USP RE45,230	
'309	USP 8,774,309	
'317	USP 8,588,317	
'768	USP 7,251,768	
'768 FH	File History for '768	2
10/850,961 FH	File History for 10/850,961	12
Andrews	Andrews, Heegard, Kozen: "A Theory of Interleavers" (1997)	7
Baltersee	Baltersee: "Achievable Rate of MIMO Channels …" (2001)	6
Caire	Caire et al.: "Bit-Interleaved Coded Modulation" (1998)	10
CFO	Carrier frequency offset	
CFO Patents	'309, '185, and '317, collectively	
CFO Provisional	U.S. Provisional Application No. 60/472,297	13
CoC	Certificate of Correction for U.S. Patent No. RE45,230	5
Data & Telecommunications Dictionary	Data & Telecommunications Dictionary (1999)	4
Defendants	Defendants and Defendant-Intervenors	
Feuersanger	Feuersanger, "An iterative Channel Estimation …" (2000)	15
HIPERLAN/2	HIPERLAN/2 Standard (2001)	16

IBM Dictionary	IBM Dictionary of Computing (10th ed. 1994)	8
IEEE Dictionary	"Authoritative Dictionary of IEEE Standard Terms" (7th ed. 2000)	9
JCC	Joint Claim Construction Statement, ECF No. 190[1]	
Ma Paper	Ma et al., "Non-Data-Aided Carrier Offset Estimators …" (2001)	14
MIMO	Multiple-input multiple-output	
Newton's	Newton's Telecommunications Dictionary (19th ed. 2003)	3
NIST	National Institute of Standards and Technology	
OFDM	Orthogonal Frequency Division Multiplexing	
Plaintiff	Plaintiff Regents of the University of Minnesota	
Plaintiff's Interrog. Responses	Plaintiff's Answers to Defendants' First Set of Common Interrogatories (Feb. 11, 2016).	11
POSITA	Person of ordinary skill in the art	
VDW	Declaration of Daniel van der Weide, Ph.D.	

[1] ECF numbers herein are in No. 0:14-cv-04666 JRT/TNL.

I. INTRODUCTION

Defendants respectfully submit this Brief in support of their proposed constructions of the disputed terms of the asserted claims. For further information on the technology underlying these patents, see the declaration of Daniel van der Weide, Ph.D. at ¶32-69. *See* ECF No. 205; 208. Section II addresses the disputed terms relating to U.S. Patent Nos. RE45,230 and 7,251,768. Section III addresses the disputed terms relating to U.S. Patent Nos. 8,774,309, 8,718,185, and 8,588,317.

II. DISPUTED TERMS IN THE '230 AND '768 PATENTS

A. Order of functions recited in the asserted independent claims of the '768 patent

Claim Number	Defendants	Plaintiff
1	To infringe claim 1, an apparatus must have components that perform the corresponding functions in each element in the order recited.	N/A
13	To infringe claim 13, a system must have a transmitter with components that perform the corresponding functions in each element in the order recited.	N/A
21	The steps of each element of the method claim 21 must be performed in the order recited.	N/A

The Federal Circuit applies a two-part test for determining whether functions recited in a claim must "be performed in the order in which they are written." *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1369 (Fed. Cir. 2003). First, the Federal Circuit "look[s] to the claim language to determine if, as a matter of logic or grammar, they must be performed in the order written." *Id*. If not, it next "look[s] to the rest of the specification to determine whether it 'directly or implicitly requires such a narrow construction.'" *Id*. at 1370 (emphasis in original).

Wi-Lan, Inc. v. Apple, Inc., 811 F.3d 455 (Fed. Cir. 2016), is illustrative of an order requirement. There, a claim directed to a "transceiver" recited a "first computing means…to ***produce modulated data symbols*** corresponding to an invertible randomized spreading of the first stream of data symbols," and "means to combine ***the*** modulated data symbols." *Id*. at 460 (emphases added). The Federal Circuit held that the producing and combining functions must be performed in order. It reasoned:

> Subsequent use of the definite articles "the" or "said" in a claim refers back to the same term recited earlier in the claim.… The term "the modulated data symbols" therefore refers back to the randomized data symbols produced by the computing means in the second claim element. Because the modulated data symbols in the second element are randomized upon being produced, those same modulated data symbols in the third element have already been randomized before they are combined. The text of the claim thus requires producing randomized symbols and then combining those randomized symbols.

Id. at 462. *See also Mantech Envtl. Corp. v. Hudson Envtl. Servs., Inc.*, 152 F.3d 1368, 1375-76 (Fed. Cir. 1998) (holding that the steps of the claimed process must be performed in order because each step required input from prior steps).

Here, like in *Wi-Lan*, each step takes as its input the output of the immediately prior step. As illustrated below, the logic and grammar of the claims requires that the steps be performed in the recited order:

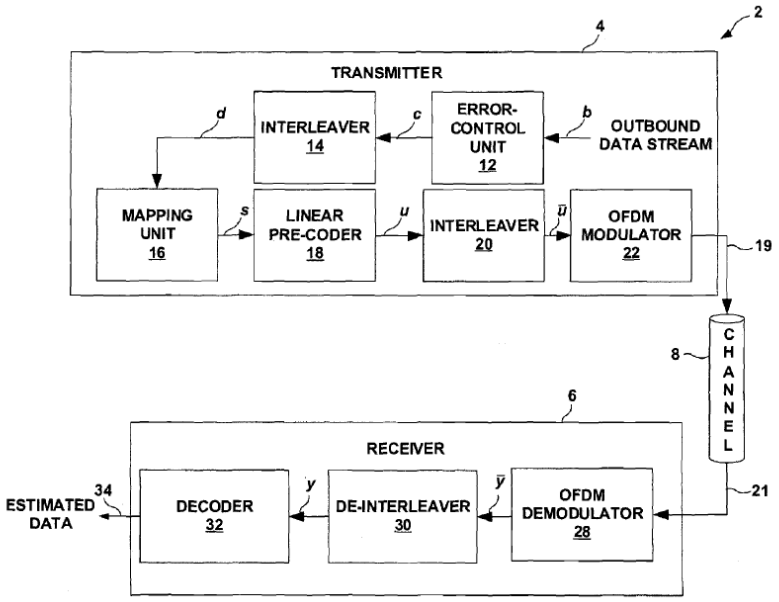
> In step [1A] ("error control coder"), an "encoded data stream" is produced.
>
> Step [1B] ("bit interleaver") must occur after step [1A], since step [1B] recites "***the*** encoded data stream," referring back to the encoded data stream produced in step [1A].
>
> Step [1C] ("mapping unit") must occur after step [1B], because "***the*** interleaved data stream" recited in step [1C] refers back to the interleaved data stream produced in step [1B].
>
> Step [1D] ("precoder") then occurs after step [1C], as step [1D] recites applying a linear transformation to "***the*** constellation symbols" to which the data was mapped in step [1C].
>
> Step [1E] ("symbol interleaver") then must occur after step [1D], because "***the*** precoded symbols" recited in step [1E] refers back to the "precoded symbols" produced in step [1D].
>
> Step [1F] ("modulator") must occur after step [1E], because step [1F] recites "***the*** permuted blocks of precoded symbols," referring back to the "permuted blocks of precoded symbols" produced in step [1E].

VDW, ¶72. The same analysis applies to claims 13 and 21, with minor distinctions. *Id*.

Defendants' construction also accords with the embodiments disclosed in the specification, confirming that it is correct. *See Wi-Lan*, 811 F.3d at 462 ("The ordering

requirement described above is consistent with the specification."). Specifically, the order in which the steps are recited in claims 1, 13, and 21 accords precisely with the order recited in the disclosed embodiment. **VDW, ¶**72. For instance, as indicated by the arrows in Fig. 1 of the '768 patent, reproduced below, a data stream undergoes error-control coding (error-control unit 12), bit interleaving (interleaver 14), mapping (mapping unit 18), precoding (linear pre-coder 18), symbol interleaving (interleaver 20), and modulation (OFDM modulator 22), in that order. **'768**, Fig. 1, 4:22-5:27.

FIG. 1



Accordingly, like in *Wi-Lan*, the claims confirm that each function recited in the independent claims of the '768 patent takes as its input, the output of the immediately preceding step, and therefore, as a matter of grammar and logic, the functions recited in the claims must be performed in the order recited.

B. "a precoder that applies a liner [sic] transformation to the constellation symbols to produce precoded symbols" ('768 cl. 1) / "a precoder that linearly precodes the constellation symbols" ('768 cl. 13) / "linearly precoding the constellation symbols by applying a linear transformation to produce precoded symbols" ('768 cl. 21)

Defendants	Plaintiff
"a precoder that applies a linear transformation to combine two or more of the constellation symbols with each other to produce precoded symbols, wherein the linear transformation has the following properties: 1) For any constellation symbols a and b, f(a + b) = f(a) + f(b) 2) For any scalar k, f(k*a) = k*f(a)"	"a precoder that applies…": a precoder that applies a linear transformation that transforms a block of input symbols into a block of output symbols in which each output symbol is a linear combination, or weighted sum, of input symbols. "linear transformation": a mathematical operation on vectors f(x), which has the property that for any vectors a and b that are valid arguments to f, f(a + b) = f(a) + f(b), and for any scalar k f(k*a) = k*f(a). A linear transformation does not include the operation of using a spreading sequence of chips, such as a Hadamard transform, to spread symbols over multiple data symbols. "constellation symbols": symbols corresponding to the characteristics of a digitally modulated signal, such as amplitude and phase

These terms are directed to the claimed linear precoding that is applied to the constellation symbols that are output by the mapping unit. The parties agree that these terms require at least the application of a linear transformation that linearly combines

multiple symbols and conforms to the two recited mathematical properties. Beyond these aspects in common, Defendants' construction is consistent with the claim language and intrinsic record, whereas Plaintiff's proposal improperly (1) reads out the claim requirement that the linear transformation be applied to "the constellation symbols," (2) expands the scope of the claims to cover non-linear transformations, even though the claims require the transformation to be linear, and (3) excludes embodiments by carving out spreading sequences and Hadamard transforms. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (*en banc*) ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction."); *Accent Packaging, Inc. v. Leggett & Platt, Inc.*, 707 F.3d 1318, 1326 (Fed. Cir. 2013) ("a claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct").

First, only Defendants' construction adheres to the claim requirement that the linear transformation be applied to "***the*** *constellation symbols*." More specifically, the claimed linear transformation must be applied to "the constellation symbols" that were output by the mapping unit. *See Wi-Lan*, 811 F.3d at 462 ("Subsequent use of the definite articles "the" or "said" in a claim refers back to the same term recited earlier in the claim.… The term "the modulated data symbols" therefore refers back to the randomized data symbols produced by the computing means in the second claim element."). That the linear precoder's input must be the constellation mapping unit's

output is consistent with, and supported by, the specification and file history. *See* **'768** at 4:44-47; *see also* **'768** FH at 164 (Applicants explained that "***the input symbols provided to the precoder***" are "***the constellation symbols output by the constellation mapping unit***."); **VDW,** ¶77-78.

Plaintiff's proposal, by contrast, enlarges the scope of the claims because it allows the linear transformation to be applied to ***any*** "block of input symbols." This could be *any* arbitrary input. Indeed, as noted below, Plaintiff's proposal would allow infringement where the linear transformation operates on symbols *other than* the output of the constellation mapping unit. Plaintiff's proposal eviscerates the claims' express requirement that the linear transformation be applied to "*the* constellation symbols," and changes the plain meaning of the claim. *See W.E. Hall Co., Inc. v. Atlanta Corrugating, LLC*, 370 F.3d 1343, 1353 (Fed. Cir. 2004)) ("Claim construction begins and ends in all cases with the actual words of the claim").

Second, although the parties seemingly agree that the claims require the application of a ***linear*** transformation, only Defendants' construction actually requires the transformation to be linear. For instance, since Plaintiff's proposal allows the linear transformation to be applied to *any* "block of input symbols" as discussed, Plaintiff's proposal would effectively allow the "linear transformation" to be non-linear. **VDW,** ¶79. Specifically, Plaintiff's proposal would allow the output of the constellation mapping unit to be put through a ***non-linear*** transformation before being fed to the linear

transformation. The combination of a non-linear operation with a linear operation can be, collectively, ***a non-linear operation***. *Id*. Thus, such a combined transformation applied to "the constellation symbols" can be non-linear. *Id.* Further, Plaintiff's proposal fails because it seeks to allow the output symbols resulting from the "linear transformation" to be a "linear combination ***or weighted sum***" of input symbols. A "weighted sum" is *not* always a linear transformation. Weighted sums can be non-linear, such as in the case of a "weighed sum of squares" operation.[2] **VDW, ¶**80. Other examples of non-linear transformations that could be combined with a linear transformation to create a "weighted sum" include taking the logarithm or taking the real and imaginary part of a complex value. *Id*. By encompassing non-linear transformations, Plaintiff's proposal contradicts the plain language of the claims. *See W.E. Hall*, 370 F.3d at 1353.

Third, Plaintiff's proposal arbitrarily excludes certain "linear transformation[s]," contradicting the claims and intrinsic record. Plaintiff seeks to exclude "spreading sequences" and "Hadamard transforms" from the scope of the claimed linear precoder. Spreading sequences and Hadamard transforms, however, can be *linear*, both as understood in the art and for meeting the pair of requirements agreed upon in the parties' constructions. **VDW, ¶**81. Indeed, if spreading sequences and Hadamard transforms did

[2] As described by NIST, this comprises squaring the input (a non-linear transformation) and then combining the squares (a linear transformation). *See* **VDW, ¶**80. As a whole, this transformation is non-linear. *Id.*

not satisfy the agreed requirements of a linear transformation, Plaintiff would not have a need to attempt to carve them out. Plaintiff's carveouts, therefore, further contradict the claims themselves. *See W.E. Hall*, 370 F.3d at 13.

Additionally, the intrinsic record not only fails to support Plaintiff's proposal, but contradicts it. The intrinsic record contains no disclaimer of spreading sequences or Hadamard transforms. *See GE Lighting Sols., LLC v. Agilight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("[D]isavowal requires that the specification or prosecution history make clear that the invention does not include a particular feature."). Additionally, at least one embodiment of the linear transformation in the intrinsic record is the very spreading matrix that Plaintiff now seeks to exclude. *See* **VDW, ¶**87. The '933 provisional, incorporated by reference into the '768 patent at 1:5-12, repeatedly describes spreading sequences as being embodiments of the claimed precoders. *See, e.g.*, '933 provisional at 6 n.1 ("***[t]he spreading matrix C can be viewed (and will be invariably referred to) as a precoder….***" (emphasis added)), 38 (using a ***spreading sequence*** as a precoder), 70 (same); *see also* **VDW, ¶**87 (explaining that the spreading matrix described in the provisional application is a spreading sequence and the claimed precoder). Thus, Plaintiff's proposal improperly reads out embodiments in the intrinsic record and should be rejected. *See Phillips*, 415 F.3d at 1316.

C. "interleaved data stream" ('768 cls. 1, 13 and 21) / "interleaved symbols" ('230 cls. 1 and 16) / "interleaved bits" ('230 cl. 49)

Defendants	Plaintiff
interleaved data stream: "bits that are the same as the bits of the encoded data stream that have been reordered so that adjacent bits are separated"	**interleaved data stream:** a data stream that is generated using an interleaver, which is an electronic circuit or computer implemented algorithm that takes an ordered set of values and reorders them"
interleaved symbols: "symbols that are the same as the encoded symbols that have been reordered so that adjacent symbols are separated"	**interleaved symbols:** "a sequence of symbols generated using an interleaver"
interleaved bits: "bits that are the same as the coded bits that have been reordered so that adjacent bits are separated"	**interleaved bits:** "a sequence of bits generated using an interleaver"

The dispute as to these terms centers on what constitutes interleaving. As compelled by the intrinsic evidence and understanding of a POSITA, Defendants' constructions require that (1) the bits or symbols be reordered so that adjacent bits or symbols are separated, and (2) the value of the interleaved bits or symbols after interleaving remain the same. By contrast, Plaintiff's proposals are overly broad because (1) they improperly encompass any form of reordering, including reordering such that adjacent bits or symbols are not separated, and (2) they are directed to a different function that changes the values of the encoded data stream. These requirements are addressed in turn, below.

First, interleaving ***requires*** the separation of every adjacent bit or symbol of the input stream. The Newton's reference, which Plaintiff cited as extrinsic evidence in connection with these terms (JCC Ex. A at 6), confirms Defendants' constructions by stating that "[i]n the interleaving process, ***code symbols are reordered before transmission in such a manner that any two successive code symbols are separated*** by l-1 symbols in the transmitted sequence, where l is called the degree of interleaving." Newton's at 415 (emphasis added); *see also* Data & Telecommunications Dictionary at 395 (interleaving for data transmission means "code symbols are arranged in an interleaved pattern before transmission and reassembled upon receipt").

An understanding of the rationale behind the interleaving in these claim terms further confirms Defendants' constructions. By way of background, interleaving is a fundamental concept to communication systems. "Interleaving" spreads apart adjacent bits or symbols to make it easier for the receiver to reconstruct received data. **VDW,** ¶43-44. There are generally two forms of interleaving, both of which are described and claimed in the '768 and '230 patents. *Id.*; **'768** at Fig. 1, 4:22-60; **'230** at Fig. 12; CoC at 7. One form of interleaving spreads bits or symbols apart ***in time***, to avoid burst errors. **VDW,** ¶43-46. The other form spreads symbols ***in frequency***, to avoid interference that affects adjacent symbols. *Id.*

The three claim terms at issue here are directed to interleaving bits or symbols ***in time***. **VDW,** ¶91. This is because, by the plain language of the claims, the "interleaved

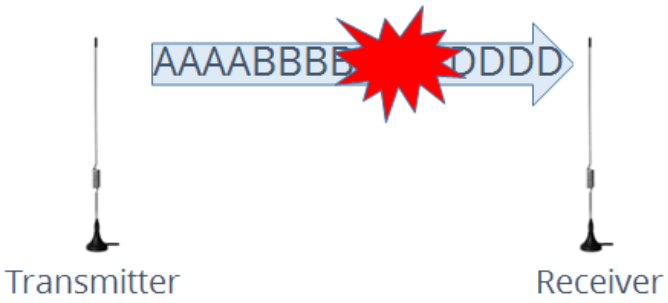
data stream," "interleaved symbols," and "interleaved bits" are created *prior to* the constellation mapping operation. *Id.* This is consistent with the intrinsic record, which describes interleaver Π_1 creating this data stream, symbols, or bits prior to constellation mapping, in contrast to a separate interleaver Π_2, which operates after constellation mapping and linear precoding and interleaves in the frequency domain. *See id.*; **'768** at Fig. 1, 4:22-60; **'230** at Fig. 12; CoC at 7.

As noted, the rationale behind interleaving in time is to avoid burst errors. In wireless communications, parts of signals may be lost in short-term interference that destroys parts of a signal before it reaches the receiver. **VDW, ¶**43-44. The loss of several adjacent bits is called a burst. *Id.* In a burst, groups of adjacent bits,[3] rather than individual bits, are lost. *Id.* A bit being impacted by a burst of noise dramatically decreases the likelihood that this bit—along with the bits transmitted just before or after it—will be received properly. *Id.*; Baltersee at 2358.

By way of illustration using letters in place of bits or symbols, if the four letters "ABCD" are sought to be transmitted, redundancy could be added to the message—*e.g.*, making it "AAAABBBBCCCCDDDD"—to help ensure that each letter reaches the

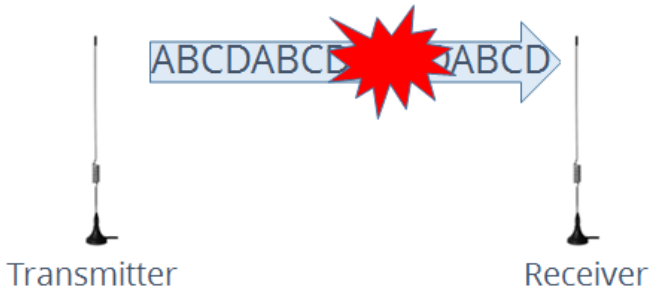
[3] For simplicity, this discussion focuses only on why bits are interleaved in time. However, the same analysis applies to why symbols are interleaved in time. **VDW**, 43-44.

receiver properly. However, a burst error could cause all transmissions of a letter to be lost, as with the letter "C" in this example:



VDW, ¶43.

Interleaving over time can solve this burst problem. The purpose of such interleaving is to "transform[] [a] bursty channel into an independently distributed channel." Baltersee at 2358; **VDW,** ¶43. That is, interleaving distributes adjacent bits or symbols across the channel in time so that if a burst occurs, previously adjacent bits or symbols will not be lost to the burst. **VDW,** ¶43-44. For example, in the prior illustration, when interleaving the letters by separating adjacent letters—*e.g.*, "ABCDABCDABCDABCD"—the same burst error does not prevent the receipt of the letter "C," as illustrated as follows:



Id.

As a result, consistent with the Newton's reference, interleaving over time ***must*** separate adjacent bits or symbols. **VDW, ¶**93. If it did not, the purpose behind these claims' calling for interleaving the data stream, symbols, or bits—avoiding burst errors—would be lost. *See AIA Eng'g Ltd. v. Magotteaux Int'l S/A*, 657 F.3d 1264, 1278 (Fed. Cir. 2011) (holding that "a construction that renders the claimed invention inoperable should be viewed with extreme skepticism").

By contrast, Plaintiff's proposals are overly broad because mere "reorder[ing]" of bits does not guarantee that they are no longer adjacent. For example, in the illustration above, Plaintiff's proposals would encompass an algorithm that simply reverses the message to read "DDDDCCCCBBBBAAAA." **VDW, ¶**95. The reversed message "DDDDCCCCBBBBAAAA" would be no less vulnerable to burst errors than the original message "AAAABBBBCCCCDDDD." *Id.* As shown in the following illustration, a single burst error could still destroy every transmission of the letter B, as was the case for the original message as explained above:

Id. Thus, a POSITA would not consider Plaintiff's proposals to be "interleaving," since it would eviscerate the very purpose behind interleaving in time. *Id.*, ¶96.

Second, the term "interleaving," as used by a POSITA, refers to the reordering of bits ***while maintaining*** the identity of each reordered bit—*e.g.*, bit 0 remains 0 and bit 1 remains 1. *See* **VDW**, ¶97. While the intrinsic record is silent on this issue, the Andrew's reference, which Plaintiff cited as extrinsic evidence pertaining to these terms (JCC Ex. A at 6), confirms Defendants' constructions by stating that an interleaver "takes symbols from an [sic] fixed alphabet as the input ***and produces the identical symbols at the output in a different temporal order***." Andrews at 1 (emphasis added). Similarly, the IBM Dictionary states that "interleave" means "to arrange parts of one sequence of things or events so that they alternate with parts of one or more other sequences of the same nature and ***so that each sequence retains its identity***." IBM Dictionary at 351 (emphasis added). Likewise, the IEEE Dictionary provides that to "interleave" means "to arrange parts of one sequence of things or events so that they alternate with parts of one or more other sequences of things or events ***so that each sequence retains its identity.***" IEEE Dictionary at 577. Additionally, the Caire reference confirms there is a "one-to-one" correspondence between the bits before and after interleaving, meaning that bit interleaving does not change the values of the bits. **VDW,** ¶97 (citing Caire at 2). Consistent with these references and the understanding of a POSITA, Defendants'

constructions are correct not to allow the bits or symbols to change in the process of being reordered by the interleaver. **VDW, ¶**97.

By contrast, Plaintiff's proposals fail because they do not require that the claimed interleaver maintain the integrity of the original values of the bits. **VDW, ¶**98. By encompassing algorithms within the scope of the claim that change the identity of the inputted bits, Plaintiff's proposals expand the claimed "interleaver" to cover completely different functions other than interleaving, such as "scrambling." *Id*. The purpose of scrambling is not to separate bits to compensate for burst errors, but rather, for example, to provide security by changing the values of the bits in a data stream. *Id*. That is, unlike interleaving, which merely rearranges bits so that adjacent bits are separated, scrambling obscures a message by, *inter alia*, reordering the bits in any fashion and even changing the identities of one or more bits. *Id*. A POSITA would consider scrambling and interleaving to be separate and distinct functions for different purposes. *Id*. As a result, Plaintiff's proposals are inconsistent with the evidence of record and understanding of a POSITA, and should be rejected.

D. "a symbol interleaver to process the precoded [symbols/data stream] to produce permuted blocks of the precoded symbols" ('768 cls. 1, 13) / "processing the [sic: precoded] symbols to produce permuted blocks of [sic: precoded] symbols" ('768 cl. 21)

Defendants	Plaintiff
"an electronic circuit or computer-implemented algorithm that takes the precoded symbols and reorders them to separate adjacent symbols"	"an electronic circuit or computer-implemented algorithm that takes an ordered set of precoded symbols and reorders them."

The parties' disputes are: (1) which symbols are interleaved, and (2) whether adjacent symbols must be separated. The intrinsic evidence supports only Defendants' construction that (1) it must be *the* precoded symbols that are interleaved, and (2) adjacent precoded symbols *must* be separated.

First, as with "the constellation symbols" in Section II.B, Plaintiff's proposal improperly reads out the claim requirement that the symbol interleaver process "***the*** precoded symbols"—*i.e.*, the symbols generated by the claimed precoder. Instead, Plaintiff's proposal calls for operating on "***an*** ordered set of precoded symbols." Plaintiff's use of "an" would allow for ***any*** ordered set of precoded symbols to be interleaved, whereas Defendants' construction remains faithful to the claim language by limiting the processing to "the precoded symbols." *See Wi-Lan*, 811 F.3d at 462 ("Subsequent use of the definite articles "the" or "said" in a claim refers back to the same term recited earlier in the claim.").

Second, only Defendants' construction correctly imposes the requirement that an interleaver separate adjacent symbols. As explained in Section II.C, the '768 patent claims interleavers that operate over time or over frequency. Unlike the interleavers described in Section II.C, the interleaver here separates symbols ***in frequency***, to avoid interference that affects adjacent symbols. **'768**, 4:65-67 ("The main role of interleaver 20, on the other hand, is to permute each block of linearly precoded symbols u ***in the frequency domain***.") (emphasis added); **VDW**, ¶103. This is because, by the plain language of the claims, this interleaver operates *after* the operations of constellation mapping and linear precoding, and will soon thereafter be mapped to frequencies. *Id.* The symbols are interleaved so that when mapped to frequencies, the adjacent symbols will not be mapped to adjacent frequencies. *Id.* This is consistent with the intrinsic record, which describes interleaver Π_2 operating after constellation mapping and precoding and interleaving symbols in the frequency domain (in contrast to interleaver Π_1, discussed above in Section II.C). *See id.*; **'768**, Fig. 1, 4:22-60; **'230**, Fig. 12; CoC at 7.

The technical rationale behind the interleaving in this claim term is to separate adjacent bits/symbols to mitigate the effects of interference on adjacent frequencies. **VDW,** ¶103. For reasons analogous to the separation of adjacent symbols over time as described in Section II.C, the interleaver here must separate adjacent symbols across frequencies in order to constitute interleaving. **VDW,** ¶103-104. That is, adjacent

symbols must be separated so groups of symbols are not lost. *Id.* Just as described in Section II.C, Plaintiff's proposal fails because it merely calls for "reordering," and thus does not ensure the separation of adjacent symbols.

E. "applying/applies a linear transformation to a/the stream of information bearing symbols" ('230 cls. 1, 16, 49, 64, 68)

Defendants	Plaintiff
"applies/applying a time invariant linear transformation to combine two or more of the information bearing symbols with each other to produce precoded symbols, wherein the linear transformation has the following properties: 1) For any constellation symbols a and b, f(a + b) = f(a) + f(b) 2) For any scalar k, f(k*a) = k*f(a)"	"transforms [transforming] blocks of symbols from a [the] stream of information bearing symbols using a linear transformation to produce symbols that linear combinations, or weighted sums, of the information bearing symbols." "linear transformation": previously construed

While the parties' constructions for these terms have several differences, one difference is critical: Defendants' construction reflects the clear and unequivocal disclaimer in the specification of the '230 patent that the claimed linear transformation must be ***time invariant***. **'230**, 5:25-30. Plaintiff's proposal, by contrast, ignores this disclaimer—allowing the transformation to be time-varying—and is therefore impermissibly broad. The Federal Circuit has held that "[w]here the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read

without reference to the specification, might be considered broad enough to encompass the feature in question." *SciMed Life Sys. v. Adv. Cardiovascular Sys.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001).

As background, a transformation is "time invariant" if the transformation does not vary as a function of time. **VDW, ¶** 107. For example, the linear transformation $y(x) = 2 \times x$ is time invariant because, at all times, *y* will equal $2 \times x$. *Id.* By contrast, the linear transformation $y(x) = 2 \times x \times t$, where t is an indication of time (*e.g.*, in minutes), varies with time based on the variable *t* and is therefore "time varying." *Id.*

In the '230 patent, Applicants clearly and unequivocally declared that the linear transformations in the claimed invention, signified by the Greek letter Θ, ***excludes*** time-varying linear transformations:

> The encoder Θ considered here does not depend on the OFDM symbol index i. ***Time-varying encoder may be useful for certain purposes***, (e.g., power loading)***, but they will not be pursued here.*** Hence, from now on, we will drop our OFDM symbol index i for brevity.

'230 at 5:25-30 (emphasis added); *see also* CoC at 9; **VDW, ¶**108. The specification is unambiguous: time-varying encoders "will not be pursued here," and as a result, the OFDM symbol index "i" will no longer appear in the specification because it is not needed. Thus, the claimed linear transformation must be time invariant.

The remainder of the '230 patent confirms this disclaimer, repeatedly and consistently describing only time-invariant linear transformations. Indeed, the disclaimer

states that the index "i," a variable indicating variations in time, would be dropped from that point forward. The matrix Θ is referenced more than 80 times after the disclaimer, and not once does it include the time variable index "i" when represented as an equation, or otherwise indicate that Θ can vary over time. **VDW, ¶**109. *See In re Abbott Diabetes Care Inc.*, 696 F.3d 1142, 1149 (Fed. Cir. 2012) ("[E]very embodiment disclosed in the specification shows an electrochemical sensor without external cables or wires…. In the case before us, however, nothing suggests or even hints that the claimed electrochemical sensor can include external cables or wires. Instead, Abbott's patents consistently show the opposite.").

Only Defendants' construction properly reflects this time-invariance disclaimer, and should be adopted. There are other differences between the parties' constructions for these terms, but they relate generally to the meaning of "linear transformation." With respect to these differences, Defendants' arguments in Section II.B apply equally here.

F. "[wherein the] linear transformation is based on multiple matrices…[]" ('230 cls. 30, 33, 40, 64, 68) / "wherein the linear transformation is based on: $\Theta=F_{N_t}^{T}$diag(1, α,…, α^{N_t-1}), $\alpha:=^{j\ 2\pi/P}$" ('230 cls. 41, 66, 70)

Claim Limitation	Defendants	Plaintiff
"[wherein the] linear transformation is based on multiple matrices [comprising]…[]"	Indefinite.	"The linear transformation can be described as multiplication by a matrix that is the product of at least two other matrices"

"wherein the linear transformation is based on: $\Theta=F_{N_t}^{T}\mathrm{diag}(1, \alpha,\ldots, \alpha^{N_t-1})$, $\alpha:=e^{j2\pi/P}$,,"	Indefinite.	The linear transformation includes a mathematical operation that can be described as multiplication by the matrix Θ as specified in the claim.

These limitations are indefinite because the linear transformation must be "***based on***" the claimed "multiple matrices" or matrix "Θ." A claim must provide "clear notice of what is claimed, thereby apprising the public of what is still open to them." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). Overturning prior precedent, the Supreme Court recently held that "claims, viewed in light of the specification and prosecution history, [must] inform those skilled in the art about the scope of the invention with reasonable certainty." *Id.*; *see also Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014). When using a term of degree, a claim, "read in light of the specification and the prosecution history, must provide objective boundaries for those of skill in the art." *Interval*, 766 F.3d at 1371. Merely identifying "*some standard* for measuring the scope of the phrase" is insufficient. *Id.* at 1370-71 (emphasis in original).

These limitations are terms of degree. "Based on" implies that the linear transformation is afforded some degree of difference from the "multiple matrices" or matrix "Θ." *See Netflix, Inc. v. Blockbuster, Inc.*, 477 F. Supp. 2d 1063, 1074 (N.D. Cal. 2007) (in pre-*Nautilus* case, "based upon the order of the list" was construed to "allow[]

for some deviation from the exact order of the list"). In this case, a POSITA cannot determine with reasonable certainty whether or not a particular linear transformation is "based on" the "multiple matrices" or matrix "Θ." **VDW, ¶**112. Neither the claims nor the intrinsic record provides any objective standard for determining how much deviation from these matrices is allowed. *See Interval*, 766 F.3d at 1370-71. The specification sets forth one example of the claimed linear transformation, but this example is unhelpful because it specifies the linear transformation to be Θ itself. *See* CoC, 6; **VDW, ¶**113; *Interval*, 766 F.3d at 1373-74 (one example in specification found insufficient for definiteness); *Geodynamics, Inc. v. Dynaenergetics US, Inc.*, No. 2:15-CV-1546-RSP, 2016 WL 6217181, at *15 (E.D. Tex. Oct. 25, 2016) (holding "substantially equal" indefinite where patent did not provide examples of embodiments that are "substantially equal"). Additionally, a POSITA would not know based on his or her background knowledge what it means for a linear transformation to be "based on" these matrices. **VDW, ¶**113. Because the boundaries of these limitations cannot be determined with reasonable certainty, these claims are indefinite. *See Interval*, 766 F.3d at 1374.

For example, claim 41 of the '230 patent requires that the precoder apply a linear transformation "based on" matrix Θ, as follows:

41. The method of claim 40, wherein the number of the antennas is represented by N_t, wherein the first matrix is based on an N_t-point inverse version of the FFT matrix, wherein the linear transformation is based on:

$$\Theta = F_{N_t}^{T} \mathrm{diag}(1, \alpha, \ldots, \alpha^{N_t-1}), \alpha := e^{j2\pi/P}$$

wherein $F_{N_t}{}^{T}$ represents the first matrix, and wherein $diag(1, \alpha, \ldots, \alpha^{N_t-1})$ represents the second matrix, wherein P is an integer.

(highlighting added). This equation specifies a linear transformation Θ using a particular variable, α, which is defined as $\alpha:=e^{j2\pi/P}$. **VDW, ¶**114. A POSITA would not be able to determine with reasonable certainty the degree to which α can differ from the claimed equation and still fall within the scope of the claim. *Id*. For example, α could be modified so that there is an 8 in the exponent instead of a 2, or so that α varies over time. *Id*. This linear transformation Θ also specifies that the first matrix must be the transpose of an FFT matrix, as denoted by the superscript "T" in F_{Nt}^{T}. *Id*. A POSITA would not be able to determine with reasonable certainty whether an equation that implemented an FFT that was not a transpose is "based on" this equation. *Id*. These would represent different equations that would provide different results, and with any of these changes to Θ, one of skill in the art would not be able to determine with reasonable certainty whether or not the claimed linear transformation is "based on" the claimed equation. *Id*.

Plaintiff's proposals, which define "based on" as "***includes*** a mathematical operation that ***can be described as*** multiplication by the matrix Θ," find no support in the '230 patent. Plaintiff simply replaces one indefinite term of degree, "based on," with another, "can be described as." The specification provides no objective standard for determining whether an operation "can be described as" the multiplication specified in Plaintiff's proposals, nor could a POSITA make such a determination with reasonable certainty. **VDW, ¶**115. It is not sufficiently clear who is doing the "describing," nor how similar an operation must be to the specified multiplication to be permissibly "described" as such. *Id.* Moreover, by using the word "includes," Plaintiff's proposals can include additional, unspecified operations, further obscuring the boundaries of Plaintiff's proposed definitions. *Id.* Thus, the claims would remain indefinite even under Plaintiff's proposals. *See Interval*, 766 F.3d at 1371 ("Even if a claim term's definition can be reduced to words, the claim is still indefinite if a person of ordinary skill in the art cannot translate the definition into meaningfully precise claim scope.").

G. "wherein the first matrix is based on a fast Fourier transform (FFT) matrix, and wherein the second matrix is based on a diagonal matrix" ('230 cls. 30, 40, 64, 68) / "wherein the first matrix is a matrix of size N_txN_t…wherein the second matrix is a diagonal matrix" ('230 cl. 33)

Claim Limitation	Defendants	Plaintiff
"wherein the first matrix is based on a fast Fourier	The term "based on" is indefinite.	Ordinary meaning

transform (FFT) matrix, and wherein the second matrix is based on a diagonal matrix" [cls. 30, 40, 64, 68]	Should the court find this term to not be indefinite, the linear transformation must be represented in the following order: [FFT matrix]* [Diagonal matrix]	
"wherein the first matrix is a matrix of size N_txN_t… wherein the second matrix is a diagonal matrix" [cl. 33]	The term "based on" in the prior limitation of this claim is indefinite. Should the court find this term to not be indefinite, the linear transformation must be represented in the following order: [first matrix of size N_t rows by N_t columns, wherein each entry of the first matrix is based on a power of $e^{j2\pi/Nt}$, each entry of a column of the first matrix being equal to one,]*[second matrix that is a diagonal matrix of size N_txN_t having diagonal entries that are based respectively on different powers of $e^{j2\pi/p}$ including the zeroth power, wherein P is a positive integer]	The first matrix is a matrix with Nt rows and Nt columns, where Nt is the number of transmit antennas in the transmitter. The second matrix is a diagonal matrix.

1. <u>The first limitation above is indefinite.</u>

The limitation "wherein the first matrix is based on a fast Fourier transform (FFT) matrix, and wherein the second matrix is based on a diagonal matrix," is indefinite for similar reasons as explained in Section II.F. Neither the claims nor the intrinsic record

inform one skilled in the art what it means for one matrix to be "based on" another matrix. *See id.*; **VDW**, ¶116.

For instance, a "diagonal matrix" is "a matrix having non-zero values only on the diagonal" (JCC at 3), such as the following:

$$\begin{matrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{matrix}$$

VDW, ¶117. Without any objective standard in the claims or specification, a POSITA would not be able to determine with reasonable certainty the degree to which a matrix can differ from this diagonal matrix and still be "based on" it. *Id.* For example, a POSITA would not know with reasonable certainty whether the following non-diagonal matrix, which adds one non-zero value outside the diagonal, falls within the scope of the claim:

$$\begin{matrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \end{matrix}$$

Id., ¶118. Alternatively, the matrix may be a tridiagonal matrix, which is a matrix that has nonzero elements on the main diagonal, as well as on the diagonals above and below the main diagonal, as in the following example:

$$\begin{matrix} 1 & 1 & 0 \\ 1 & 1 & 1 \\ 0 & 1 & 1 \end{matrix}$$

Id. The specification does not provide an objective standard for determining whether these other matrices are "based on" a diagonal matrix. *Id*., ¶119. As a result, this limitation renders the claims indefinite. *See Interval*, 766 F.3d at 1371.

2. If the Court does not find these terms indefinite, the matrices must be multiplied in the recited order.

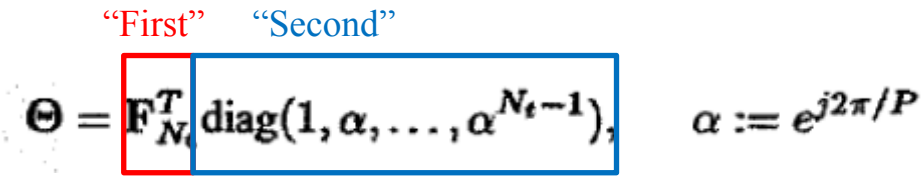
In the event the Court determines these claims are not indefinite, there would be no dispute that the recited "linear transformation" in these claims is represented by multiplying together the claimed "first" and "second" matrices. The parties disagree as to the required *ordering* of the matrices in this multiplication. Only Defendants' construction recites the intended ordering.

Matrix multiplication is not commutative; the product of two matrices can be dependent upon the order in which the matrices are multiplied. **VDW**, ¶120. Thus, A*B (A times B) does not necessarily equal B*A (B times A). *Id.*

To one skilled in the art, a mathematical expression is read from left to right. *Id*., ¶121 If a mathematical expression includes matrices identified as the "first" and "second," one skilled in the art would have understood that the "first" matrix appears first (on the left) and the "second" matrix appears second (on the right). *Id*. This understanding is important, since reversing the order of matrices in a multiplication may provide a different result. *Id*.

Under the plain meaning of the claims, the multiplication must be carried out in the following order: ["first matrix"] * ["second matrix"]. *Id.*, ¶120. Defendants' constructions reflect this ordering, whereas Plaintiff's proposals do not.[4] *Id.*

This understanding is confirmed by the intrinsic record. As Plaintiff concedes, the intrinsic record's only disclosure of the matrix multiplication in these limitations places the "first matrix" (the FFT matrix or matrix of size N_txN_t) on the left and the "second matrix" (the diagonal matrix) on the right, as follows:



See Provisional App. No. 60/374,935 at 47 (annotated), 59 (same); CoC at 6 (same); **VDW,** ¶122; Plaintiff's Interrog. Responses, Ex. B at 33, 37, 69, 103, 109 (admitting that this equation is the only support for the first limitation above. Defendants' ordering is further confirmed by claims 41, 66, and 70 of the '230 patent, which depend on claims 40, 64, and 68 at issue here. These claims set forth the same equation for Θ and refer to $F_{N_t}^{T}$, situated on the left side of the multiplication, as the "first" matrix and *diag*(1, α,…, α^{N_t-1}), situated on the right side of the multiplication, as the "second" matrix. Thus,

[4] Defendants' construction for the transformation in claim 33, while appearing lengthy, simply substitutes in the actual claim language for the recited "first" and "second" matrices directly from the claim itself.

Defendants' constructions are consistent with not only the claim language but also the only embodiment. *See Gen. Am. Transp. Corp. v. Cryo-Trans, Inc.*, 93 F.3d 766, 770 (Fed. Cir. 1996) (construing limitation consistent with the embodiment because it was "not just the preferred embodiment of the invention; it is the only one described").

H. "applying a unitary matrix" ('230 cls. 3, 18, 46, 56)

Defendants	Plaintiff
"performing a mathematical operation that, when expressed in its matrix form, is multiplication by a unitary matrix"	"performing a mathematical operation that, when expressed in matrix form, includes multiplication with at least a unitary matrix"

Defendants' construction properly requires a showing that the mathematical operation, when expressed in its matrix form, is multiplication by a unitary matrix, whereas Plaintiff's proposal is overly broad because virtually ***any*** mathematical operation meets Plaintiff's definition. Thus, Plaintiff's proposal eviscerates this limitation altogether. *See Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950-51 (Fed. Cir. 2006) ("When the language of a claim is clear, as here, and a different interpretation would render meaningless express claim limitations, we do not resort to speculative interpretation based on claims not granted.").

As background, the parties have agreed that a "unitary matrix" is "a square matrix whose conjugate transpose is equal to its inverse." JCC at 3. This means that, for any unitary matrix U, multiplying U by its conjugate transpose, U^*, yields the identity matrix,

I. **VDW**, ¶124. That is, *UU** = *I*. *Id.* Additionally, a matrix multiplied by the identity matrix is itself. *Id.* Thus, for a matrix *A*, *AI* = *A*. *Id.*

Plaintiff's proposal fails because it would allow Plaintiff to argue that any mathematical operation includes multiplication with at least a unitary matrix. For example, consider a system that multiplies two non-unitary matrices, *A* and *B*. One of ordinary skill in the art would recognize that this operation, *AB*, would not fall within the scope of the term at issue, "applying a unitary matrix," because the operation is a multiplication of purely non-unitary matrices. **VDW**, ¶125. For the reasons discussed, however, *AB* is the mathematical equivalent of *ABUU** (which equals *ABI*, which equals *AB*). *Id.* Thus, Plaintiff's proposal allows virtually any operation to be arbitrarily manipulated to cause this term to be met, rendering the limitation meaningless. *Id.*

Defendants' construction, by contrast, differs from Plaintiff's proposal by including "its" and not including "at least." This clarifies that the actual algorithm must, when written in its matrix form, be multiplication by a unitary matrix. **VDW**, ¶126. It is undisputed that it is proper to express a mathematical operation in "its matrix form," since Plaintiff agreed to such a construction for the term "linear precoder comprises a unitary matrix." Thus, using the example above, Defendants' construction makes clear that *AB* cannot be arbitrarily manipulated to *ABUU** to satisfy the limitation. *Id.* Defendants' construction is consistent with how a POSITA would interpret this term. *Id.*

Finally, Plaintiff's proposal would render other claim language superfluous. Claims 18, 46, and 56 of the '230 patent provide that the linear transformation "comprises applying a unitary matrix." Plaintiff's inclusion of "at least" in the construction for this term would render "comprises" superfluous. *See Dippin' Dots, Inc. v. Mosey*, 476 F.3d 1337, 1343 (Fed. Cir. 2007) ("the term 'comprising' raises a presumption that the list of elements is nonexclusive.").

I. "wherein P is an integer" ('230 cls. 41, 66 and 70)

Defendants	Plaintiff
"wherein P is a positive integer"	None of the terms in this phrase require construction. The jury can apply the ordinary meaning of the phrase.

The parties dispute whether the variable integer "P" must be positive. While the claims do not indicate whether "P" is positive or negative, the specification defines "P" as unambiguously positive. *See* CoC at 4, 6; *Phillips*, 412 F.3d at 1313 (a POSITA "is deemed to read a claim term…in the context of the entire patent, including the specification").

Claims 41, 66, and 70 of the '230 patent claim a particular equation for the linear transformation, as follows:

> *70. The device of claim 68, wherein the linear transformation is based on:*
>
> $$\Theta = F_{N_t}^{T} \operatorname{diag}(1, \alpha, \ldots, \alpha^{N_t-1}), \alpha := e^{j2\pi/P}$$

The specification sets forth this same equation, as follows:

> LCP-B provides a construction of unitary precoders for any number of transmit-antennas $N_t \in \mathrm{N}$:
>
> $$\Theta = \mathbf{F}_{N_t}^{T} diag(1, \alpha, \ldots, \alpha^{N_t - 1}), \quad \alpha := e^{j2\pi/P}$$
>
> where $P \in \mathrm{N}$, and $\mathbf{F}_{N_t}$ is the N_t-point inverse fast Fourier transform (IFFT) matrix whose $(m,n)st$ entry is given by $N_t^{-1/2} \exp(j2\pi(m-1)(n-1)/N_t)$. Notice that this LCP matrix amounts to phase-rotating each entry of the symbol vector $\mathbf{s}$, and then modulating in a digital multicarrier fashion that is

CoC at 6 (highlighting added).

In the context of this claimed equation, the specification defines P by stating that "P ∈ N." *Id.* To a POSITA, this means the value of P must be chosen from among the values in the set N. **VDW, ¶129.** The set N is explicitly defined in the specification as the "***positive*** integer set," as follows:

> Let ^{T} and ^{H} represent transpose and conjugate transpose, respectively; Tr(·) denotes trace; $[\cdot]_{mn}$ denotes the (m,n)th entry of a matrix; $\mathbf{I}_{N_t}$ denotes an $N_t \times N_t$ identity matrix; $diag(d_1,\ldots,d_P)$ denotes a diagonal matrix with diagonal entries $d_1,\ldots,d_P$; N, Z, Q, R, and C stand for the positive integer set, the integer ring, the rational number field, the real number field, and the complex number field, respectively; j denotes $\sqrt{-1}$.

CoC at 4 (highlighting added). The intrinsic record sets forth no other definition for either P or N. Because P must be chosen from only positive numbers, P must be positive. *See Phillips*, 415 F.3d at 1316 (where the specification reveals "a special definition given to a claim term…, the inventor's lexicography governs").

J. "a diagonal matrix to phase-rotate each entry of a symbol vector" ('230 cls. 30, 40, 64, 68)

Defendants	Plaintiff
"a diagonal matrix that applies a set of phase offsets to the entries of a symbol vector, such as diag(1, α,…, αNt-1)"	"a diagonal matrix that applies a set of phase offsets to the entries of a symbol vector, such as diag1, α, …, αNt-1, to modify the phase of at least some of those symbols"

This term calls for "a diagonal matrix to phase-rotate each entry of a symbol vector." As background, a "diagonal matrix" is a matrix that has non-zero values only along the diagonal from upper-left to lower-right, as in this example:

$$\begin{matrix} A & 0 & 0 \\ 0 & B & 0 \\ 0 & 0 & C \end{matrix}$$

In this example, the diagonal consists of variables A, B, and C. **VDW, ¶**131.

In the context of this term, the values on the diagonal represent a phase-rotation to be applied to each symbol. *Id.* Thus, applying the matrix in the example above, the first symbol is phase-rotated by a factor associated with A, the second symbol by a factor associated with B, and the third symbol by a factor associated with C. *Id.*

With respect to the construction of this term, the parties agree insofar as a diagonal matrix applies a set of phase offsets to the entries of a symbol vector. Plaintiff, however, seeks to shoehorn in a further requirement—*i.e.*, that the phase of at least some symbols in the symbol vector be *modified*. Plaintiff's proposal has no basis in, and contradicts, the

claim and intrinsic record. This term calls for the diagonal matrix merely to *phase-rotate* each entry of a symbol vector. Contrary to Plaintiff's proposal, this does not mean that the phase of even a single entry in the symbol vector must be *modified*.

Rather, as demonstrated throughout the intrinsic record, to "phase-rotate" an entry in the symbol vector includes not modifying its phase at all. For example, this term appears in claim 30 of the '230 patent. Claim 31, which depends from claim 30, is as follows:

> *31. The wireless communication device of claim 30, wherein the number of the antennas is represented by N_t, wherein the first matrix is based on an N_t-point inverse version of the FFT matrix, wherein the linear transformation is based on:*
>
> $$\Theta = F_{N_t}^{T} \, \mathrm{diag}(1, \alpha, \ldots, \alpha^{N_t-1}), \alpha := e^{j2\pi/P}$$

The entries within the parenthesis of the diagonal matrix in claim 31 are the phase-rotations to be applied to each symbol in the symbol vector. **VDW**, ¶133; *see also* CoC at 6 (describing the embodiment of claim 31 as "amount[ing] to phase-rotating each entry of the symbol vector…."). The phase-rotation applied to the first symbol is "1," which means that the phase of the first symbol is not modified. **VDW**, ¶133. Because this term calls for phase-rotating "each" entry in the symbol vector—including the first symbol—the claims of the '230 patent plainly do not require that "phase-rotating" a symbol means modifying the symbol's phase. *Id.*, ¶132. As a result, there is nothing in the claim term

to support Plaintiff's proposal that even one symbol's phase be modified. *See W.E. Hall Co., Inc. v. Atlanta Corrugating, LLC*, 370 F.3d 1343, 1353 (Fed. Cir. 2004)) ("Claim construction begins and ends in all cases with the actual words of the claim.").

K. "subcarriers carry different linear combinations of the information symbols" ('230 cls. 2, 17)

Defendants	Plaintiff
"subcarriers carry different linear combinations of the stream of information symbols transformed by the second encoder"	"the different subcarriers carry different weighted sums of the stream of information symbols transformed by the second encoder"

The parties dispute whether the claim term "linear combination" should be replaced with the term "weighted sum." It should not. As described in Section II.B, a weighted sum can be the result of either a linear *or* non-linear combination. Thus, Plaintiff's proposal broadens this term to encompass systems that perform non-linear transformations, and should be rejected. **VDW**, ¶135.

III. DISPUTED TERMS IN THE CFO PATENTS

A. "null subcarrier" (CFO Patents, all asserted claims)

Defendants	Plaintiff
"A subcarrier on which no value is intended to be transmitted during a specific time period, used to estimate carrier frequency offset"	"A subcarrier on which no value is intended to be transmitted during a specific time period"

There is no dispute that a "null subcarrier" is a subcarrier on which no value (*i.e.*, a "zero symbol," *see* **'317**, 2:30-32) is intended to be transmitted during a specific time-period. Where the parties disagree is whether *every* zero symbol is a "null subcarrier." As explained below, and consistent with the intrinsic record and how the claimed invention is intended to operate, Defendants' construction properly limits "null subcarriers" to the subset of zero symbols that are used to estimate CFO, whereas Plaintiff's overbroad proposal encompasses zero symbols that are expressly *not* "null subcarriers."

Critically, the CFO Patents explain that there are at least *two different types* of zero symbol transmissions, but define only *some* of these zero symbols to be "null subcarriers." Specifically, the CFO Patents expressly distinguish (1) zero symbols used to remove interference from other channels and(2) zero symbols that serve as a null subcarrier:

> In each OFDM transmission block, there are four non-zero training symbols, 4 zero symbols to remove interference from other channels, and one zero symbol serving as a null subcarrier.

'317, 15:63-67.[5] Thus, the CFO Patents' description of "null subcarriers," which expressly does *not* include all zero symbols, compels Defendants' construction.

[5] The CFO Patents further state that training symbols—which are expressly distinct from null subcarriers—"may include both non-zero symbols and zero symbols."

Plaintiff's proposal would improperly sweep every zero symbol into the definition of "null subcarrier."

Correctly recognizing that only *some* zero symbols are "null subcarriers," Defendants' construction properly states that null subcarriers are just those zero symbols that are used to estimate CFO. The only use described in the CFO patents for null subcarriers is performing CFO estimation, and the only way the CFO Patents describe performing CFO estimation is by using null subcarriers. *See, e.g.*, **'317,** 8:35-38 ("The null subcarrier is inserted so that the position of the null subcarrier hops from block to block and enables CFO estimation to be separated from MIMO channel estimation."); 2:30-36; 14:10-18; 10/850,961 FH, Response to 9/30/10 OA at 16 ("The 'hopping' of Applicant's claims, however, is based upon the insertion of null subcarriers at different positions within two or more individual blocks (*e.g.*, OFDM blocks), where carrier frequency offset estimation is performed based on the positions of these null subcarriers in the blocks.").

More specifically, the CFO Patents explain that null subcarriers—again, a special subclass of "zero symbols"—are inserted at different positions in each block, in accordance with a hopping code. *Id.* at 2:30-36, 8:9-38. This is depicted in the example representation below, where the colored dots represent data values on subcarriers and the

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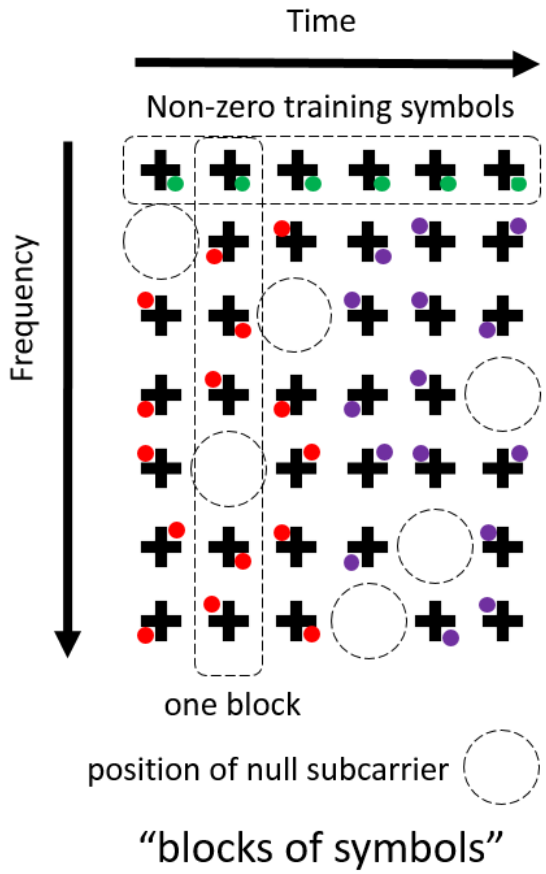
'317, 2:27-28; *see also, e.g., id.* at cl. 1 (training symbols and null subcarriers are inserted separately, and are thus distinct).

dashed circles represent the inserted null subcarriers (which have no data values) at the transmitter *before* transmission:

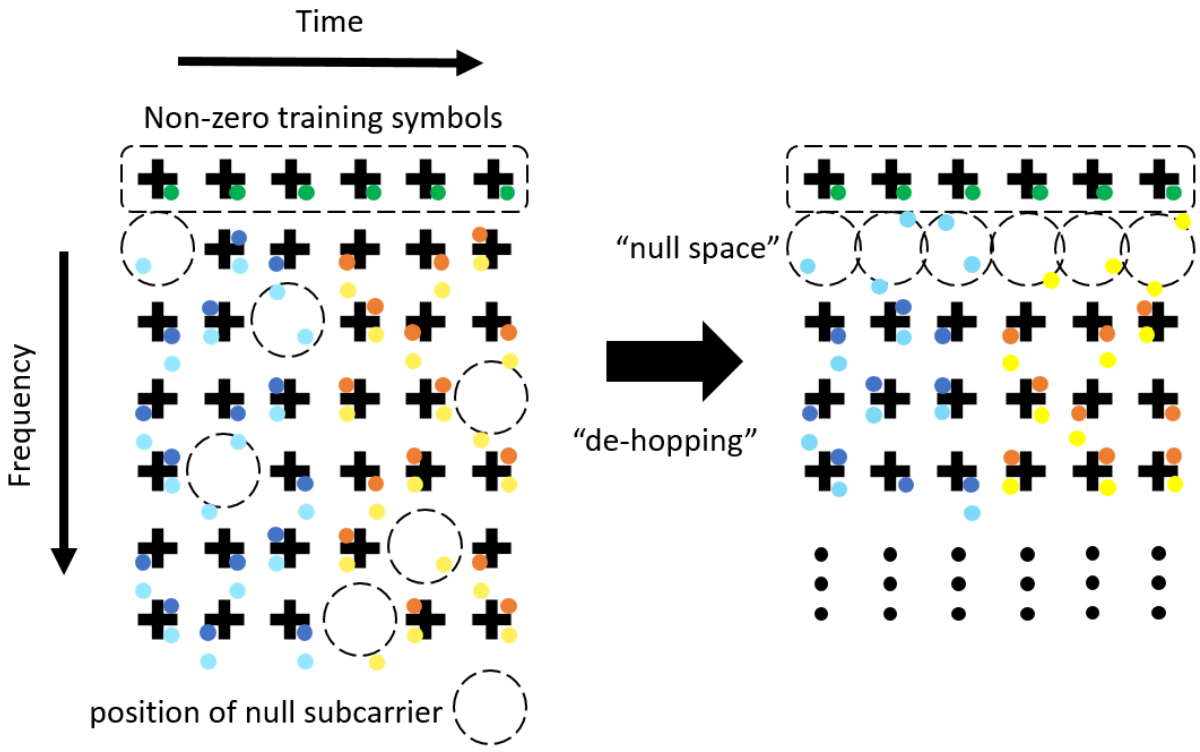


VDW ¶157.

According to the CFO Patents, CFO causes these zero symbols to be received differently than how they were transmitted, where data values become "offset" from their intended frequency, including some data values being shifted into the frequencies of the null subcarriers. **'317** at 9:37-38; **VDW** ¶66. The CFO Patents teach that the receiver

"de-hops" the null subcarriers and estimates CFO based on measurement of any shift of data values into the null space, with the goal of minimizing a "cost function". **'317** at 9:38-39; 10:27-28; 14:9-11.

This is depicted in another illustrative example below, this time representative of a transmission as received by a receiver *after* transmission. The left-hand figure includes lighter colored dots representing the "offset" of data values caused by CFO, including offsets into the null subcarriers. The right-hand figure represents the realignment of the null subcarriers used for CFO by "de-hopping" to create a null space:



VDW, ¶159.

Finally, after the receiver estimates CFO, the null subcarriers are removed, and then channel estimation is performed. **'317**, 14:15-22, Fig. 4 (steps **60** and **62**); *see also* CFO Provisional, 3-4 ("To estimate the channels, we first take FFT of $\bar{y}_v(k)$ and then remove the null-subcarrier at the receiver….").

Thus, the CFO Patents describe not only using the null subcarriers for the sole purpose of estimating CFO, but also removing the null subcarriers after estimating CFO, confirming that they cannot be used for any other purpose. *See id*. Only Defendants' construction properly limits the construction for "null subcarrier" to the zero symbols that are used to estimate CFO. *See Phillips*, 415 F.3d at 1316 ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.").

Indeed, if Plaintiff's proposal were adopted, the CFO Patents would not be able to fulfill their stated purpose. Plaintiff's proposal would allow infringement to be shown by the presence of *any* zero symbols that otherwise satisfy the claims, even if those zero symbols were not used to estimate CFO. Since the only technique described to estimate CFO is to use zero symbols that are "null subcarriers," allowing null subcarriers not to serve the purpose of estimating CFO would leave the claims without ***any*** way to allow estimation of CFO. **VDW**, ¶142. But as is made clear throughout the CFO Patents, allowing CFO (and channel) estimation is the very purpose of the claimed invention. *E.g.*, **'317**, 2:16-20 ("In general, the invention is directed to techniques for carrier

frequency offset (CFO) and channel estimation of [OFDM] transmissions over [MIMO] frequency-selective fading channels."), 3:57-59 ("FIGS. 5-12 are graphs illustrating performance estimates of the CFO and channel estimation techniques described herein."); *see also, e.g., id.* at Title, Abstract, 4:18-21. Under Plaintiff's proposal, the alleged invention would not be usable for its own alleged purpose. *See AIA Eng'g Ltd. v. Magotteaux Int'l S/A*, 657 F.3d 1264, 1278 (Fed. Cir. 2011) (holding that "a construction that renders the claimed invention inoperable should be viewed with extreme skepticism").

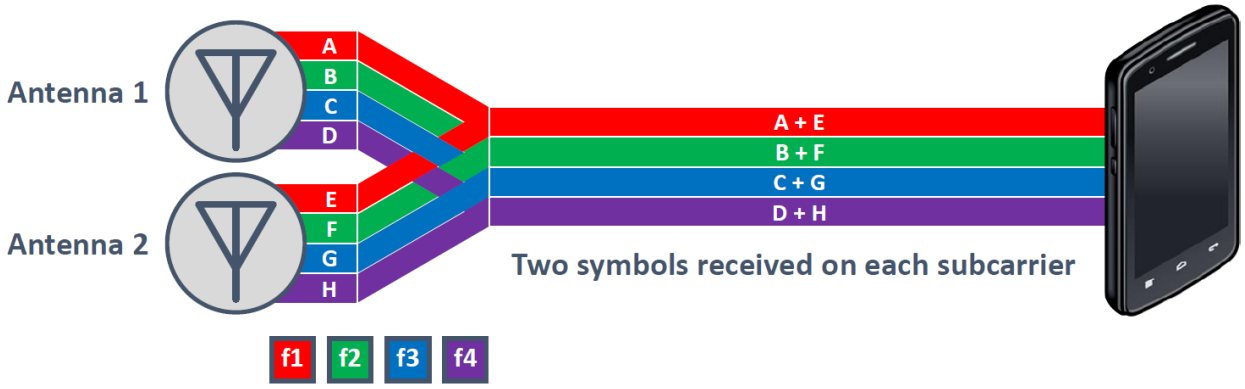
B. "subcarrier" (CFO Patents, all asserted claims)

Defendants	Plaintiff
"In a MIMO multi-carrier waveform, one of a number of carrier frequencies within a larger frequency band"	"In a multi-carrier waveform, one of a number of carrier frequencies within a larger frequency band"

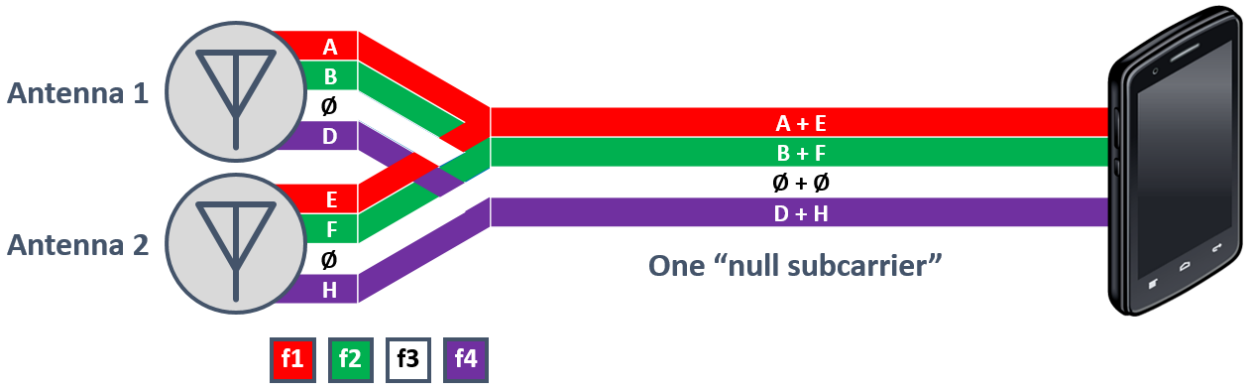
The term "subcarrier" does not appear in the claims of the CFO Patents as a standalone term, but rather in the context of the parties' proposed constructions for "null subcarrier," above. In this context, it is undisputed that, at a minimum, a subcarrier must be, "[i]n a multi-carrier waveform, one of a number of carrier frequencies within a larger frequency band." However, as discussed below, and as only Defendants' construction makes clear by including "MIMO," to qualify as a "null subcarrier," the zero symbol must be present at a subcarrier across all antennas—otherwise a non-zero value will be

transmitted on that frequency. To the extent Plaintiff's proposal does not impose such a requirement, it should be rejected for being inconsistent with the specification and preventing the claimed system from operating as disclosed.

As is made clear from the intrinsic record, the CFO Patents are directed to MIMO systems, meaning that there are multiple antennas at the transmitter and receiver. *See*, *e.g.*, **'317**, 2:16-20, Abstract, Title. Indeed, ***each and every*** embodiment of "the invention" relates to a MIMO system. **'317,** 17:33-38 ("Various embodiments of the invention have been described. The invention provides techniques for carrier frequency offset (CFO) and channel estimation of [OFDM] transmissions over multiple-input multiple-output (MIMO) frequency-selective fading channels."). In a MIMO system, the waveform transmitted through the channel consists of the combined output from all of the transmitter's antennas. **VDW**, ¶68. As soon as each antenna transmits a signal, those signals instantly combine into a single waveform. **VDW**, ¶68. This is shown in the demonstrative below with respect to an exemplary two-antenna MIMO transmitter, where each transmit antenna transmits two symbols over one subcarrier (*e.g.*, C + G over subcarrier f3, in blue):

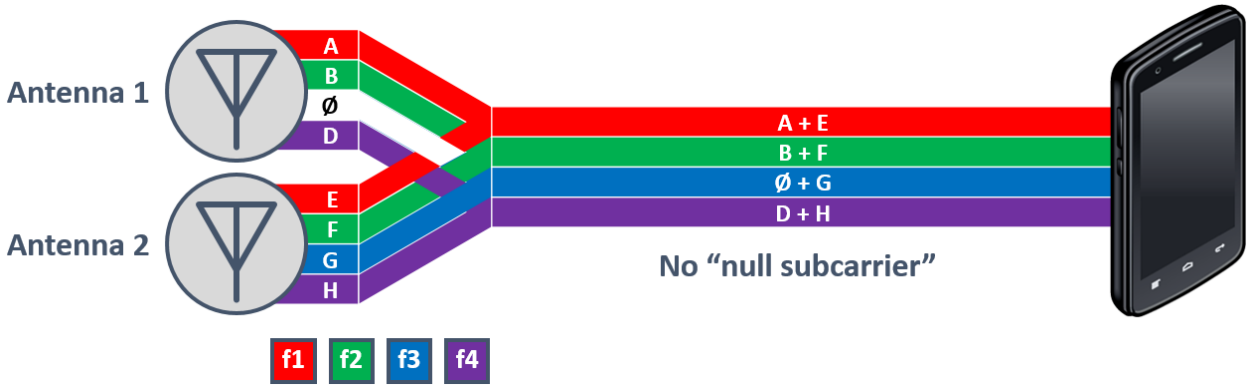


As explained, the CFO Patents describe that the receiver performs CFO estimation using null subcarriers. *See* Section III.A. In particular, the receiver estimates CFO based on measuring the shift of data values into the null space caused by CFO. *Id.* To allow the receiver to make this measurement, the transmission on that subcarrier must be null. **VDW**, ¶151-2. To ensure this null transmission, the transmitter must transmit a zero symbol at that subcarrier across every antenna. *Id.* This is depicted in the demonstrative below, where zero symbols are transmitted simultaneously from both antennas on the same subcarrier (*e.g.*, Ø+Ø over subcarrier f3, white):



In this manner, the CFO patents allow the receiver to determine the shift of data values into the "null subcarrier," *e.g.*, from either the purple or the green subcarriers, due to carrier frequency offset, thereby enabling CFO estimation. **VDW** ¶151. This approach is also consistent with the specification, which states that the number of zero symbols that are removed after CFO estimation is equal to N_t, which is the total number of antennas at the transmitter. *Id.*; **'317**, 10:36-54. That is, by transmitting a null at that subcarrier on every antenna, a total of N_t zero symbols are transmitted. *See id.*; *see also id.* at 8:16-18 ("Applying the hopping code given in equation (8) inserts a zero symbol referred to as a null subcarrier in each block $\tilde{u}_{\mu}(k)$."). Thus, Defendants' clarification (within the context of the construction for "null subcarrier") properly ensures that a "null subcarrier" is a zero symbol across all antennas. *See Phillips*, 415 F.3d at 1315-16.

By contrast, allowing a "null subcarrier" to include a *non-null* transmission on the same frequency, but from a different antenna, would be contrary to the disclosed invention. **VDW**, ¶152. Specifically, if one or more antennas of a transmitter were to send a transmission on a subcarrier that was *not* null, the transmitter's combined waveform for that subcarrier would, in turn, be non-null. *Id.* As a result, for that subcarrier, the receiver would receive a signal that was not null. *Id.* As shown below, for example, where a zero symbol (Ø) is transmitted from antenna 1 on frequency f3, but a non-zero symbol (G) is transmitted over the same subcarrier (f3) on antenna 2, the entire subcarrier will be non-null (Ø+G):



Thus, due to the presence of the transmitted data value, symbol "G", the receiver would be unable to detect the shift of other data values from either the green or purple subcarriers, as the CFO Patents require for CFO estimation. *See id.*; **'317**, 9:37-39, 9:55-67, 10:27-31, 14:27-37. Thus, to the extent Plaintiff's proposal for "subcarrier" allows the claimed "null subcarrier" to have a non-zero value on one or more antennas by not including the key clarifying word "MIMO," the construction should be rejected because the claimed system would not function as disclosed. *See AIA*, 657 F.3d at 1278.

C. "form … blocks of symbols/output symbols" "forming blocks of symbols/output symbols" (CFO Patents, all asserted claims)

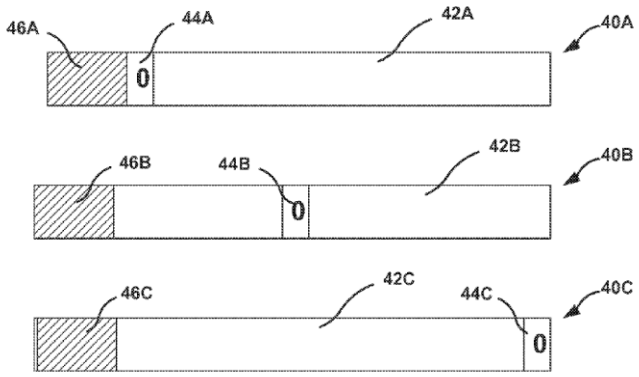
Defendants	Plaintiff
"Generating 'blocks of symbols' for transmission at consecutive times"	The terms "form" and "forming" do not require construction. The jury can apply the ordinary meaning of those terms.

The parties agree that "block of symbols" should be construed as "a group of symbols for transmission at a given time." Thus, the only issue in dispute is whether the

asserted claims require generating these "blocks of symbols" for transmission at consecutive times. They do.

As captured by Defendants' construction, the specification uniformly describes the technique for forming blocks of symbols as creating ***consecutive*** blocks for transmission. **'317**, Fig. 3; 8:18-20; 13:23-28. In contrast, Plaintiff seeks to avoid a construction altogether, inappropriately hiding behind an undisclosed "ordinary meaning" for this term. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008) ("When the parties raise an actual dispute regarding the proper scope of these claims, the court, not the jury, must resolve that dispute.").

Figure 3 and its accompanying description is the *only* disclosure of the "formation" of blocks of symbols in the specification:



'317, Fig. 3. Specifically, Figure 3 "illustrates example transmission blocks **40**A, **40**B, and **40**C generated by transmitter **4** of communication system **2**." *Id.* at 13:23-25. Critically, the specification states that "transmission blocks **40**A, **40**B and **40**C

correspond to ***consecutive*** transmission blocks $\bar{u}_u(k)$ **16**… with block index k=0, k=1, and k=2, respectively." *Id.* at 13:23-28 (emphasis added). This unambiguous statement makes clear that the blocks of symbols are generated for transmission at consecutive times, in accordance with Defendants' construction.

Moreover, the CFO Provisional makes clear that Figure 3 of the specification is not a mere embodiment, but rather *the* description (indeed, the ***only*** description) of the formation of "blocks of symbols" pursuant to the claimed invention. *See Absolute Software, Inv. v. Stealth Signal, Inc.*, 659 F. 3d 1121, 1136-1137 (Fed. Cir. 2011) ("[I]n some circumstances, a patentee's consistent reference to a certain limitation or a preferred embodiment as 'this invention' or the 'present invention' can serve to limit the scope of the entire invention, particularly where no other intrinsic evidence suggests otherwise."). In particular, the CFO Provisional states that the "scheme" of the alleged invention is to "form" a series of consecutive output blocks by inserting training symbols into each block, as follows:

In summary, our scheme can be summarized as follows:

1) After obtaining the information blocks $\{\mathbf{c}_\mu\}_{\mu=1}^{N_t}$ corresponding to the N_t transmit-antennas, we first insert N_t training symbols to form $\mathbf{b}_\mu(k) = [\mathbf{0}_{1\times(\mu-1)}, b, \mathbf{0}_{1\times(N_t-\mu)}]^T$. The position of these training symbols is fixed from block to block. The structure of $\bar{\mathbf{u}}_\mu(k)$ is depicted in Fig. 2.
2) We insert one zero per block in a position that hops from block to block with hop-step $N/(L+1)$.
3) We perform MIMO-OFDM at both transmitters and receivers.
4) We de-hop first the received block and then we estimate ω_ν as in (13).

CFO Provisional, 3 (emphasis added). This passage further states that the resulting structure is depicted in Figure 2 of the CFO Provisional, which, like Figure 3 of the CFO Patents, depicts three transmission blocks that are consecutive as shown by their consecutive block indices k=0, k=1, and k=2:

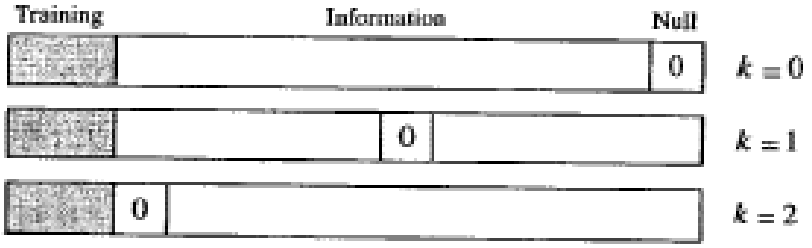


Fig. 2. One example of $\bar{\mathbf{u}}_\mu(k)$ structure

CFO Provisional, Fig. 2; *see* **'317**, 13:23-28. Consequently, the CFO Provisional confirms that "forming" blocks of symbols means generating blocks of symbols for transmission at ***consecutive*** times.

Additionally, the CFO Patents' equations for hopping and de-hopping codes and the cost function require that blocks of symbols be generated for transmission at consecutive times. **VDW**, ¶155. This requirement is imposed by the equations' use of the index "k"—representing consecutive transmissions of blocks—throughout the description of the claimed system. *See, e.g.*, **'317**, 8:18-20 ("Dependence of T_{sc} on the block index k implies that the position of the inserted null subcarrier changes from block to block."); 13:25-27. The claimed invention nowhere discloses or enables any other type of "forming," as 35 U.S.C. § 112(1) requires. Since no other type of "forming" is enabled by the specification, the patent cannot claim any such invention—and if it did, the claims would be invalid as lacking enablement. *See In re Wright*, 999 F.2d 1557, 1561 (Fed. Cir. 1993) ("[T]o be enabling, the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation.'").

It is not surprising that the "formed" blocks of symbols are consecutive, since the claimed system would not operate otherwise. If blocks were not "formed" consecutively, the system would be unable to distinguish data values in the null space caused by CFO from other data values—*i.e.*, data values in blocks that do not have null subcarriers. **VDW**, ¶158; *see also* "Ma Paper." As discussed above (*see* Sections III.A and III.B), the system estimates CFO by determining how much the data values shifted, by virtue of the offset, into the null space. If the null space is not actually null—that is, if it is

purposefully contaminated by subcarriers with data values—the system will not operate as described because it will not be able to distinguish the offset from the contamination, and therefore it cannot attempt to minimize the CFO through the disclosed "cost function." **VDW**, ¶158. *See AIA*, 657 F.3d at 1278 (holding that "a construction that renders the claimed invention inoperable should be viewed with extreme skepticism").

In sum, Defendants' construction is compelled by the intrinsic record.

D. "block length" ('317 cls. 1, 19)

Defendants	Plaintiff
"The number of subcarriers in a block of symbols"	"The number of symbols in a block"

"position" or "positions" (CFO Patents, all asserted claims)

Defendants	Plaintiff
"Frequency range"	"The location of a symbol in a block of symbols"

Because "block length" and "position[s]" are related terms that refer to the general structure of OFDM block transmissions in the specification, Defendants brief the terms together for convenience. As noted above, the parties agree that "blocks of symbols" refers to "a group of symbols for transmission at a given time." The disputes here turn on whether, in the context of the specification, (1) the term "block length" means the number

of the subcarriers within a block (Defendants) as opposed to merely the number of symbols in a block (Plaintiff), and (2) the term "position" means a frequency range (Defendants) or merely the locations of symbols in a block of symbols (Plaintiff).

First, only Defendants' construction for "block length" is supported by the intrinsic record. The CFO Patents repeatedly define "N" as expressing "block length," with "N" being the number of subcarriers in a block of symbols. For example, the specification explicitly dictates that "[t]he OFDM block length is designed as N=64 as in HIPERLAN/2." **'317**, 15:26-32. The HIPERLAN/2 Standard, referenced in the CFO Patents, defines block length as the number of subcarriers, meaning "N" refers to 64 subcarriers. *See* Feuersanger at 1-3; HIPERLAN/2 Standard; *see also* **VDW**, ¶165. The CFO Patents confirm that "N" corresponds to a number of subcarriers, not merely a number of symbols. **'317**, 14:39-45 ("Similarly, the signal-to-noise ratio (SNR) versus CRLB decreases as the number of blocks increases. If N>>N−K, i.e. ***the number of subcarriers*** is much greater than the number of null subcarriers, $T_{zp} \approx I_N$."). Thus, the specification defines "block length" as N and "N" as **the number of subcarriers in a block of symbols**.

Second, Defendants' construction for "position" is supported by the specification, which, in describing the channel estimation and CFO mitigation techniques of the prior art, explains that "[i]n the IEEE 802.11a, IEEE 802.11g, and HIPERLAN/2 standards, sparsely placed pilot symbols are present in every OFDM symbol and pilot symbols are

placed in the same positions from block to block." *See* **'317,** 1:60-64. In each of those systems, the "positions" within a block correspond to ***specific carrier frequency ranges***. *See* Feuersanger at 1-3; HIPERLAN/2 Specification; *see also* **VDW**, ¶169. Similarly, the CFO Provisional describes that the "position" of training symbols is fixed from block to block as depicted in Fig. 2. CFO Provisional, 3. In Figure 2 of the CFO Provisional, reproduced above (Section III.C), the "position" of the training symbols changes along the frequency domain over time. **VDW**, ¶170.[6] Each of these "positions" corresponds to a range in frequencies within a larger band. **VDW**, ¶170-1. Thus, the intrinsic record dictates that "position[s]" refers to a frequency range.

[6] In discussing prior art during prosecution of the parent application to the CFO Patents, Applicants also explained the meaning of "position." Specifically, Applicants described the prior art at issue (US 2004/0166887 – "Laroia") as follows: "[t]he pilots change their positions, or "hop," over time for various reasons such as frequency diversity." 10/850,961 FH, Resp. to Sept. 30, 2010 OA at 14. Figure 8 from Laroia makes clear that over time, the disclosed pilots occur at different frequency ranges. **VDW**, ¶171.

E. "a training symbol insertion module configured to…[up to 'wireless communication channel']" ('317 cl. 19)

Defendants	Plaintiff
This claim term is governed by § 112(6) **Function:** form blocks of symbols by inserting training symbols within two or more blocks of information-bearing symbols [and] applies a hopping code to each of the blocks of symbols to insert a null subcarrier at a different position within each of the blocks of symbols, wherein the hopping code causes a position of the null subcarrier to change from block to block, wherein the position change caused by the hopping code is based, at least, on a block length and a cyclic prefix length, wherein the cyclic prefix length is based, at least, on an amount of multipath propagation in the wireless communication channel **Structure:** training symbol insertion unit 15 implementing equations (5) and (8)	"training symbol insertion module": an electronic circuit or computer-implemented algorithm that places training symbols within blocks of information-bearing symbols

This term is governed by 35 U.S.C. §112(6) as it recites a function without reciting a definite structure. *See Williamson v. Citrix Online LLC*, 792 F.3d 1339, 1349-51 (Fed. Cir. 2015) (*en banc*) (overturning strong presumption that a limitation lacking the word "means" is not subject to §112(6)).

In *Williamson*, the Federal Circuit construed the term "distributed learning control *module*" as invoking §112(6) without the word "means," noting that "'[m]odule' is a

well-known nonce word that can operate as a substitute for 'means' in the context of § 112, para. 6." 792 F.3d at 1350. The court also found that the prefix, "distributed learning control," did not impart any "structural significance" to the term. *Id.* at 1351.

Similarly here, "training symbol insertion module" invokes §112(6), because the claim phrase is recited in functional language, and the claim provides no structure corresponding to that function. Neither "training symbol insertion," "module," nor the rest of the term provides any structural significance—it merely recites function. **VDW**, ¶174. Additionally, the claim element is drafted in traditional means-plus-function format:

> a training symbol insertion *module configured to form* blocks of symbols by inserting training symbols within two or more blocks of information-bearing symbols, wherein the training symbol insertion *module applies* a hopping code...

In other words, the claim merely replaces the term "means for forming" with "*module configured to form*" and "means for applying" with "*module applies*" in reciting the two functions performed by the "training symbol insertion module."

As in *Williamson*, the term "module" is a nonce word in the claim and does "not provide any indication of structure because it sets forth the same black box recitation of structure for providing the same specified function as if the term 'means' had been used." *See* 792 F.3d at 1350; *see also Ranpak Corp. v. Storopack, Inc.*, 168 F.3d 1316 (Fed. Cir. 1998) (unpublished) ("term 'settable control module' invokes section 112 paragraph 6,

because it merely sets forth the same black box without recitation of structure for providing the same specified function"). Moreover, the prefix "training symbol insertion" does not impart any structural significance; although the specification of the CFO Patents describes a training symbol insertion unit **15**, the specification fails to impart any structural significance to that term. *See* **'317**, Fig. 2, 5:32-57, 7:43-8:51. Nor would a POSITA understand "training symbol insertion module" to define specific structure.[7] **VDW**, ¶173.

Additionally, the remainder of the claim recites no structure that would carry out the two claimed functions. **VDW**, ¶174. Therefore, the term "training symbol insertion module" must be "construed to cover the corresponding structure …. described in the specification and equivalents thereof." *See* 35 U.S.C. §112(6); *Williamson*, 792 F.3d at 1350. "A structure disclosed in the specification qualifies as a 'corresponding structure' if the specification or the prosecution history 'clearly links or associates that structure to the function recited in the claim.'" *Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1311 (Fed. Cir. 2012).

Here, the corresponding structure in the specification is the training symbol insertion unit **15** implementing equations (5) and (8). **'317**, 5:32-57, 7:43-56; **VDW**,

[7] Plaintiff's proposal confirms the lack of structure for this term: "electronic circuit" and/or "computer implemented algorithm" are generic and provide no guidance. **VDW**, ¶174. This vague proposal illustrates that "training symbol insertion module" does not recite definite structure and, therefore, must be construed under §112(6).

¶176. More specifically, as the CFO Patents explain, "[e]ach of training symbol insertion units **15** inserts two or more training symbols, which may have non-zero or zero values, within space-time encoded blocks $\{c_\mu(k)\}_{\mu=1}^{Nt}$ **14**…." **'317**, 5:32-57. The CFO Patents state:

> The insertion of the training symbols is performed in two steps.
>
> In the first step, each of training symbol insertion units **15** inserts a block of training symbols $b_\mu(k)$ into the corresponding block of information bearing symbols $c_\mu(k)_{\mu=1}^{Nt}$ **14** in accordance with equation (5)….
>
> In the second step, N−K zeros are inserted per block $\tilde{u}_\mu(k)$ to obtain $\bar{u}_\mu(k)$. This insertion can be implemented by left-multiplying $\tilde{u}_\mu(k)$ with the hopping code T_{sc} given in equation (8).... Applying the hopping code given in equation (8) inserts a zero symbol referred to as a null subcarrier in each block $\tilde{u}_\mu(k)$.

'317, 7:43-56, 8:9-18.

Training symbol insertion unit **15** implementing equations (5) and (8) is the only recitation of structure in the specification to perform the claimed function, and thus should be found to be the corresponding structure here under §112(6).

F. "inserting at least one training symbol adjacent to at least one null subcarrier" ('185 cls. 6, 15; '309 cls. 5, 19)

Defendants	Plaintiff
"Inserting, within a block, at least one training symbol at an adjacent frequency to at least one null subcarrier"	"inserting at least one training symbol adjacent to at least one null subcarrier": placing at least one training symbol next to at least one null subcarrier

This term, present only in dependent claims, requires insertion of a training symbol "adjacent to" a null subcarrier. However, the term is silent as to, and parties dispute, the context in which the training symbol and null subcarrier must be "adjacent." Only Defendants' construction is consistent with the claims, including the claims from which they depend, and the specification, in that it properly clarifies that the insertion must be ***at an adjacent frequency within a block***. Plaintiff's proposal, on the other hand, fails to capture the meaning of "adjacent" in the context of the claims and could be interpreted, untethered to the specification, as symbols on the same frequency, but transmitted in different blocks close in time.

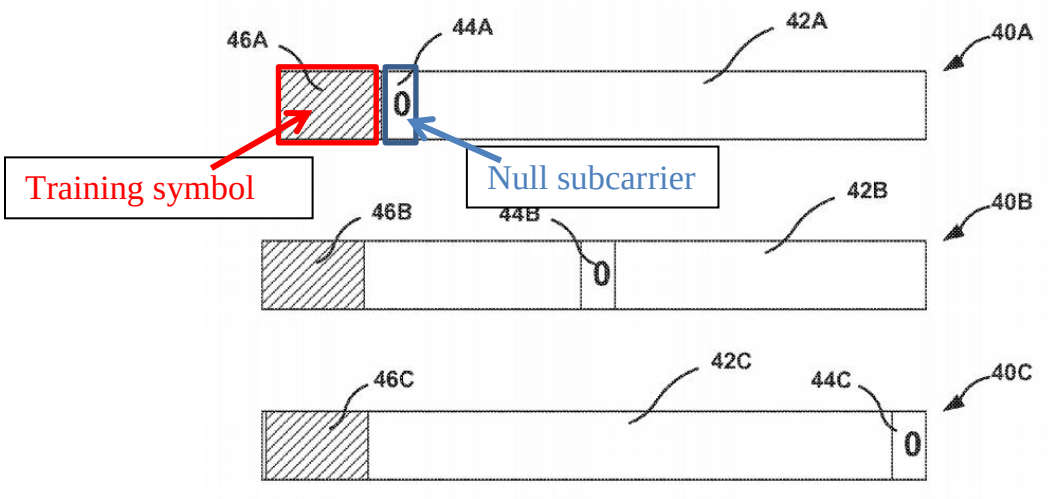
Importantly, each independent claim from which these claims depend requires, among other things, (1) *forming blocks* of information-bearing symbols and (2) *inserting*

training symbols and null subcarriers *within* these blocks.[8] The independent claims' requirements of "forming" and "inserting" means that *the blocks* of information-bearing symbols must first be *formed*, and then the training symbols and null subcarriers are *inserted* into those blocks. *See* **'317**, 2:37-43, 5:32-43; *see also* CFO Provisional, 3 ("*After obtaining the information blocks*..., we first insert N_t training symbols...."). The disputed claim limitation—in the dependent claims—further limits *how* the at least one training symbol and at least one null subcarrier are inserted *within a block*. *See* Section III.B. ("Subcarrier"). Specifically, at least one training symbol and at least one null subcarrier are inserted *within a block at subcarriers adjacent to each other in that block*. *Id.* Each block is a one-dimensional vector spanning multiple ***frequencies*** at a given time (*i.e.*, one symbol (data value or a zero-value) per subcarrier, by the number of subcarriers in the block). **VDW**, ¶180. And, since subcarriers are frequencies (in the block of frequencies), the insertion is at an *adjacent frequency*.

In addition to the claim language, the specification confirms Defendants' construction. For example, the specification describes—and depicts with reference to Figure 3 (below)—the transmissions blocks described by these claims. Specifically,

[8] *See, e.g.*, **'309**, cl. 1 ("*forming* two or more *blocks* of output symbols ... wherein the *forming* comprises encoding two or more blocks of information-bearing symbols for transmissions over the two or more antennas, and *inserting* training symbols and null subcarriers *within* the two or more blocks of information-bearing symbols at positions determined by a hopping code"); *see also* **'309**, cl. 16; **'185**, cls. 1, 9.

"transmission blocks **40A**, **40B**, and **40C** correspond to consecutive transmission *blocks* $\bar{u}_{\mu}(k)$ ***16*** ... [wherein] *each transmission block* **40A-40C** includes space-time encoded information bearing symbols **42A-C**, null subcarriers **44A-44C**, and training symbols **46A-46C**, respectively." **'317**, 13:23-31; *see also* **CFO Provisional**, Fig. 2 (same).



CFO Patents, Figure 3 (annotated)

Thus, although each of transmission blocks **40A**, **40B**, and **40C** (above) satisfies the independent claim requirements of (1) forming blocks of information bearing symbols and (2) inserting training symbols and null subcarriers into those blocks, *only* transmission block **40A** satisfies the disputed *dependent limitation* of "inserting at least one training symbol [**46A**] ***adjacent to*** at least one null subcarrier [**44A**]."

Thus, because the claims require that training symbols and null subcarriers be inserted into each *block*, and because each block is one-dimensional spanning multiple *frequencies*, the disputed limitation of the dependent claims requires "inserting, *within a*

block, at least one training symbol at an *adjacent frequency* to at least one null subcarrier."

Defendants' construction is true to both the claims, read as a whole, and the intrinsic record. Plaintiff's proposal, however, is untethered to either and impermissibly attempts to broaden the claims to allow for the mere "placing" of at least one training symbol "next to" at least one null subcarrier, unrestricted to being "adjacent to" each other within the blocks of information-bearing symbols each is required to be "inserted."

G. "training symbol" (CFO Patents, all asserted claims)

Defendants	Plaintiff
"symbol with a predefined value that can be used by the device that receives the symbol to determine a physical characteristic of the transmitted signals"	"In a transmission system, a symbol having a predefined value that is transmitted by the transmitter to enable a receiver to determine a parameter that can be used to decode other transmitted symbols."

Defendants accepted the very construction for "training symbol" that Plaintiff originally proposed to the Court. JCC at 31. Plaintiff, however, subsequently proposed a new construction the day before opening briefs were due. The dispute now is whether the training symbol is strictly limited to being used for decoding (Plaintiff) or not

(Defendants), and whether the training symbol is strictly limited to the "transmission system" (Plaintiff) or not (Defendants).

The intrinsic record is clear and compels Defendants' construction. The CFO Patents consistently describe using a training symbol to determine one or more physical characteristic of the transmitted signals. For example, the specification describes using training symbols to determine CFO, channel interference, channel estimation, and phase noise. *See, e.g.*, **'317**, 2:16-3:26, 4:22-47, 14:9-32, 15:60-16:9, (describing using training symbols to determine CFO and channel interference); 7:37-52, 8:32-51, 16:22-54, (estimating CFO), 12:48-60 (using training symbols to estimate phase noise); 17:1-12 (using training symbols to estimate CFO, channel estimation, and phase noise).

Plaintiff's proposal is also flawed to the extent it would exclude almost all of the preferred embodiments discussed above. *Accent Packaging, Inc. v. Leggett & Platt, Inc.*, 707 F. 3d 1318, 1326 ("[A] claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct."). For example, the specification describes using certain training symbols to determine CFO—a characteristic of the transmitted signals—***not*** to decode. *Supra* Section III.A (explaining that null subcarriers, a class of training symbols, are ***exclusively*** used for CFO estimation). While it is true that each of the steps taken at the transmitter and receiver may ultimately assist in decoding, because decoding is typically the final step in the transmission process, inserting "used for decoding" into every step in transmission and reception is senseless,

particularly where every claim except one does not require decoding. **VDW**, ¶184. Finally, Plaintiff's proposal limits training symbols to a "transmission system," a term that never appears in the specification, and appears to exclude the receiver, contrary to every disclosed embodiment. *E.g.*, **'317**, 2:2-4. Defendants' construction, on the other hand, is true to the intrinsic record and should be adopted by the Court.

Dated: March 16, 2017

Respectfully submitted,

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